REMARKS

Applicant respectfully requests the Examiner's consideration of the present application, as amended.

Summary of Office Action

Claims 37-60 are pending.

The request for Declaration of Interference has not been decided.

The Petition to Correct the Filing Date has been acknowledged.

Claims 37, 43, 48, and 58 were rejected under 35 U.S.C. § 112, second paragraph.

Claims 37-60 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,085,526 of Sawtell, et al. ("Sawtell") in view of U.S. Patent No. 5,560,017 of Barrett, et al. ("Barrett") and further in view of U.S. Patent No. 5,255,149 of Matsuo ("Matsuo").

Summary of Amendments

Claims 49, 51, 54, and 58 have been amended. Applicant respectfully submits that support for the amendments is found in the specification including the claims as originally filed and the drawings. Applicant respectfully submits that the amendment to claims 49, 51, 54, and 58 does not add new matter.

Statement of Prior Art

The Examiner has cited U.S. Patent No. 5,422,832 of Moyal ("Moyal") as being "prior art made of record...considered pertinent to applicant's disclosure." (12/27/96 Office Action, p. 6).

Applicant respectfully submits that U.S. Patent No. 5,422,832 has a filing date of December 22, 1993. The present application has a priority date of September 21, 1993, i.e., more than three months prior to the filing date of the Moyal patent. Thus applicant respectfully submits that Moyal *is not prior art* with respect to the present application.

Response to rejection under 35 U.S.C. § 112, second paragraph

Claims 37, 43, 48, and 58 were rejected under 35 U.S.C. § 112, second paragraph.

With respect to claims 37, 43, and 48 the Examiner has rejected the use of the word "register" as being vague. In particular, the Examiner has stated:

> Is the register rom, prom, or ram, etc. memory[?] In claim 37, 43, the register is storing a threshold temperature, while in claim 48 it is being programmed by the processor unit. Are the registers in the first two claims rom and the last ram, prom or some other programmable memory? Since the last register is being programmed by the processor.

(12/27/96 Office Action, p. 2)

Applicant respectfully submits that the register stores a value that corresponds to a threshold temperature. Registers are not properly referred to as ROM, RAM, PROM, etc.

The use of the terms "ROM," "RAM," or "PROM" implies devices that have address lines, data lines, and control signals for accessing a particular cell or groups of cells within an array of memory cells.

Registers have data output lines and control signal lines. If the register is programmable it must also provide for data input. Neither programmable nor nonprogrammable registers have address lines.

The term "register" is often used in the computer arts. Typically a value stored elsewhere in memory (e.g., ROM, RAM, etc.) must be placed into a register before the value can be operated upon.

Applicant respectfully submits that claim 48 depends from claim 43, not claim 37. Claim 43 includes the language "a register storing a register value corresponding to a threshold temperature." Claim 47 includes the language "wherein the processor unit programs the register with another register value" Applicant respectfully submits that claim 47 properly adds additional structure to claim 43 and is not inconsistent with claim 43.

With respect to claim 58, the Examiner has stated:

> As per claim 58, the step of driving the clock signal at an "intermediate" frequency if the threshold signal is asserted and the first threshold is deasserted is vague. To what reference is the frequency "intermediate"?

(12/27/96 Office Action, p. 3)

As stated above, applicant has amended claim 58. Amended claim 58 does not include such language. To the contrary, amended claim 58 includes the language

> 58. The method of claim 54 wherein step d) further comprises the steps of:
>
> i) *driving the clock signal at a first frequency* if neither the first threshold signal nor the second threshold signal are asserted; and
>
> ii) *driving the clock signal at a second frequency* if the first threshold signal is asserted and the second threshold signal is not asserted, *wherein the second frequency is less than the first frequency.*

(Claim 58, as amended)(*emphasis added*)

Applicant respectfully submits that the relationship between the first and second frequencies is properly set forth in amended claim 58.

Applicant respectfully submits that the Examiner's rejections under 35 U.S.C. § 112 have been overcome.

Response to 35 U.S.C. § 103 rejections

Claims 37- 60 were rejected under 35 U.S.C. § 103 as being unpatentable over Sawtell in view of Barrett and Matsuo.

With respect to the rejection of claim 37, 39, 40, 41, 42, 59 and 60 the Examiner has stated:

> The Barrett patent, however discloses a system with clock frequency controller responsive to interrupt and software loop repeatedly executing instructions to slow down the system clock, specifically clock circuitry (Fig. 2, #26, summary of the invention), a register storing a register value corresponding to a threshold temperature (Fig. 4, #56, #58, #60, col. 5 lines 30-50), a processor unit coupled to the clock circuitry...The Barrett patent also teaches that power consumption and heat generation can be reduced by decreasing the speed of the system clock (col. 2, lines 1-5). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Sawtell with those of Barrett to produce a microprocessor that can change it's clock speed and threshold temperature according it's heat requirement using a programmable thermal sensor.

(12/27/96 Office Action, p. 4)

The Examiner made a similar statement with respect to claims 43-48 and based the rejection of claims 49-57 on the previous statements with respect to Barrett (12/27/96 Office Action, pp. 5-6).

Applicant respectfully traverses the Examiner's characterization of Barrett. First, the described registers are *external* to the microprocessor, thus the microprocessor does not comprise them even if Barrett and Sawtell are

combined. Moreover, the registers disclosed in Barrett do not store register values corresponding to threshold temperatures of the microprocessor as asserted by the Examiner.

Although Barrett discloses that decreasing the speed of the system clock reduces power consumption and heat generation, Barrett does not teach reducing the clock in response to the heat generation or power consumption. To the contrary, Barrett discloses reducing the clock speed in response to detected wait states and increasing the clock speed in response to detected interrupts *irrespective of the temperature of the microprocessor.* Referring to Fig. 4 of Barrett, the registers store values corresponding to clock frequencies (#58, 58, 62) or values for disabling speed switching interrupts (#60) (Barrett, col. 5, lines 30-52, col. 6, lines 17-41; Fig. 4, #56, 58, 60, 62). These values determine *when* the clock signal frequency can be switched and *what frequency* the clock signal will be switched to *wholly independently of the temperature of the microprocessor.*

Applicant respectfully submits claims 37-60 are patentable under 35 U.S.C. § 103 in view of Sawtell, Barrett, and Matsuo, alone or in combination.

Sawtell includes a disclosure of a three terminal programmable temperature detector apparatus that may be integrated on a single semiconductor chip. A first terminal is coupled to a power supply through a single non-precision resistor. A second terminal receives a ground reference. A third terminal provides an indication of an object's temperature crossing a selected temperature transition point. The temperature transition point is determined by the value of the resistor. (Sawtell, col. 2, lines 25- 63; col. 3, lines 30-40).

Barrett includes a disclosure of a clock controller for controlling the system clock frequency of a CPU. The clock control circuitry is external to the CPU (Barrett, col. 4, lines 25-44; Figure 2). The system clock frequency is reduced during system wait states and immediately returns the system clock to a normal frequency in response to any condition that signals a need for a higher frequency (Barrett, col. 2, lines 32-42). Wait events (such as a keystroke wait), and interrupt acknowledges are sensed in order to vary the clock frequency. In particular, the system clock is slowed in response to wait states and increased to normal in response to interrupts (Barrett, col. 2, lines 43-57). An application program may initiate a wait cycle in a BIOS routine to periodically set the system clock at a reduced frequency. The BIOS software causes the clock control circuit to return the system clock to the normal frequency once an awaited event occurs. (Barrett col. 2, lines 59-64). Barrett further discloses using software executed by the processor to write the normal frequency into a register that can be read by the interrupt responsive circuitry.

Matsuo includes a disclosure of an electronic apparatus that includes a temperature abnormality detector. The electronic apparatus includes a heat generating element. A plurality of temperature sensors are coupled to the heat generating element which is powered by a power supply (Matsuo, col. 3, lines 20-56; Fig. 1). When one of the sensors fails the other sensor is used to permit continuous monitoring of the temperature of the heat generating element. Two checks are used to determine if a sensor failed. (1) If a sensor does not indicate a temperature within a first range of temperatures possible to achieve, the sensor is presumed to have failed. (2) If a sensor indicates reaching T2 without reaching T1 when T1<T2, the sensor is presumed to

have failed (Matsuo, col. 4, lines 38 thru col. 5, line 35). The temperature abnormality detector provides a signal to indicate failure of a sensor and switches to another sensor to provide continuous monitoring of the temperature of the electronic apparatus (Matsuo, col. 4, lines 38-45; col. 6, lines 13-20; Fig. 3). The power supply to the heat generating element is interrupted if the temperature of the heat generating element actually reaches a high temperature (i.e. T2). (Matsuo, col. 6, lines 13-36). A control unit including a microprocessor controls the power off signals and the failed sensor signal. (Matsuo, col. 5, line 47 thru col. 6, line 12).

Applicant respectfully submits none of Sawtell, Barrett, and Matsuo, alone or combined, teaches or discloses *a microprocessor comprising 1) a register storing a register value corresponding to a threshold temperature, or 2) a programmable thermal sensor receiving the register value, wherein the programmable thermal sensor generates a first interrupt signal if the microprocessor temperature exceeds the threshold temperature.*

To the contrary, as stated by the Examiner, Sawtell discloses a programmable thermal sensor but does not teach or disclose a register, clock circuitry or a processor (12/27/96 Office Action, p. 4). Moreover, applicant submits that Sawtell does not teach or disclose incorporating the programmable thermal sensor within a microprocessor. Thus *Sawtell does not teach or disclose a microprocessor comprising registers or programmable thermal sensors.*

With respect to Matsuo, a heat generating element and temperature abnormality detector are incorporated within an electronic apparatus, but the temperature abnormality detector is not located within a microprocessor.

To the contrary, the temperature abnormality detector comprises a microprocessor within its control unit. The temperature sensors are coupled to measure the temperature of the heat generating element, not the microprocessor. The microprocessor is distinct from the heat generating element. (Matsuo, Figs. 1-2).

Moreover, the temperature abnormality detector is not programmable. To the contrary, Figure 2 clearly illustrates the source of instructions for the microprocessor is ROM 10. "The temperature data is subjected to *predetermined* processing and discrimination in accordance with a program written in ROM 10." (Matsuo, col. 4, lines 1-5). Given that ROM is an acronym for "Read Only Memory," applicant submits that Matsuo's thermal abnormality detector is not programmable. *Thus applicant respectfully submits Matsuo does not teach or disclose a microprocessor comprising a programmable thermal sensor.*

Finally, applicant respectfully submits Matsuo does not teach or disclose a register storing a register value corresponding to a threshold temperature (of the microprocessor). Even if one inferred from Figure 3 that registers are used at some point to store the "first level" and "second level" temperatures, the "first level" and "second level" values correspond to the temperature of the heat generating element, not that of the microprocessor. *Thus Matsuo does not teach or disclose a microprocessor comprising the claimed register storing a register value corresponding to the threshold temperature.*

With respect to Barrett, applicant respectfully submits that Barrett does not teach or disclose a programmable thermal sensor. Although Barrett

discloses that the heat generated by the system can be reduced by slowing the clock, Barrett does not teach or disclose measuring the heat to vary the clock frequency. To the contrary, Barrett teaches reducing the clock frequency in response to detected wait states irrespective of the temperature of the microprocessor. The clock frequency is increased in response to interrupts irrespective of the temperature of the microprocessor. *Thus Barrett does not teach or disclose a microprocessor comprising a programmable thermal sensor.*

With respect to the registers cited by the Examiner, applicant respectfully submits that the described registers are *external* to the microprocessor. (Barrett, col. 4, lines 25-42; Fig. 2). Moreover, contrary to the Examiner's assertion that Barrett's registers store register values corresponding to a threshold temperature (12/27/96 Office Action, p. 4, 5) applicant submits that the cited registers store 1) clock frequency values or 2) values for enabling clock frequency switching. (Barrett, col. 5, lines 30-50; Fig. 4, #56, 58, 60, 62). *Thus Barrett does not teach or disclose a microprocessor comprising a register storing a register value corresponding to a threshold temperature.*

Thus applicant respectfully submits that none of the cited references, alone or combined, teaches or discloses *a microprocessor comprising 1) a register storing a register value corresponding to a threshold temperature, or 2) a programmable thermal sensor receiving the register value, wherein the programmable thermal sensor generates a first interrupt signal if the microprocessor temperature exceeds the threshold temperature.*

In contrast, claims 37 and 43 include the language:

37. *A microprocessor comprising:*

a register storing a register value corresponding to a threshold temperature;

a programmable thermal sensor receiving the register value, wherein the programmable thermal sensor generates a first interrupt signal if a microprocessor temperature exceeds the threshold temperature corresponding to the register value;

clock circuitry for providing a clock signal for the microprocessor; and

a processor unit coupled to the clock circuitry, wherein the processor unit executes instructions to vary the frequency of the clock signal in response to the first interrupt signal.

(Claim 37)(*emphasis added*)

43. A computer system comprising:

an active cooling device;

a microprocessor comprising:

a register storing a register value corresponding to a threshold temperature;

a programmable thermal sensor receiving the register value, wherein the programmable thermal sensor generates a first interrupt signal if a microprocessor temperature exceeds the threshold temperature, wherein the active cooling device is activated in response to the interrupt signal.

(Claim 43)(*emphasis added*)

Thus applicant respectfully submits claims 37 and 43 are patentable under 35 U.S.C. § 103 in view of the cited references.

With respect to claim 59, applicant respectfully submits that none of the references, alone or combined, teaches or discloses *a microprocessor comprising means for varying the frequency of the microprocessor clock signal in response to at least one of a first and second signal, wherein the first signal is generated if the microprocessor temperature exceeds a first threshold level and a second signal is generated if the microprocessor temperature exceeds a second threshold level.*

To the contrary, applicant respectfully submits Sawtell does not teach or disclose measuring the temperature of a microprocessor, providing first and second signals when a microprocessor temperature exceeds a first threshold and a second threshold, or means for varying the frequency of a microprocessor clock in response to such first and second signals.

Matsuo provides for a multiple threshold levels, but the threshold levels represent temperature of the heat generating element, not the microprocessor. Moreover, Matsuo does not teach or disclose means for varying the frequency of the microprocessor clock in response to these threshold levels.

Although Barrett discloses varying the frequency of the microprocessor clock signal, the "means" for varying the clock frequency is located *externally* to the microprocessor. Moreover, the "means" varies the frequency of the clock signal in response to detected wait states and interrupts - *not temperature.* Thus Barrett does not teach or disclose a microprocessor comprising means for varying the frequency of the microprocessor clock signal in response to at least one of a first and second signal, wherein the first signal is generated if the microprocessor temperature exceeds a first threshold level and the second signal is generated if the microprocessor temperature exceeds a second threshold level.

Thus applicant respectfully submits that none of the references, alone or combined, teaches or discloses *a microprocessor comprising means for varying the frequency of the microprocessor clock signal in response to at least one of a first and second signal, wherein the first signal is generated if the microprocessor temperature exceeds a first threshold level and a second*

signal is generated if the microprocessor temperature exceeds a second threshold level.

In contrast, claim 59 includes the language:

> 59. A microprocessor comprising:
> a processor unit;
> a clock circuit providing a clock signal to the processor unit, the clock signal having an associated frequency;
> *a thermal sensor generating a temperature signal corresponding to a temperature of the microprocessor;*
> logic circuitry coupled to the thermal sensor, *the logic circuitry generating a first signal if the temperature signal exceeds a first threshold level and a second signal if the temperature signal exceeds a second threshold level;* and
> *means for varying the associated frequency of the clock signal in response to at least one of the first and second signals.*

(Claim 59)(*emphasis added*)

Thus applicant respectfully submits that claim 59 is patentable under 35 U.S.C. § 103 in view of the cited references.

With respect to claims 49, 51, and 54 applicant respectfully submits that none of Matsuo, Barrett, or Sawtell teaches or discloses *a method of controlling a temperature of a microprocessor including the step of generating a temperature signal within the microprocessor indicative of the temperature of the microprocessor.*

To the contrary, Sawtell discloses a programmable thermal sensor. Although Sawtell teaches integrating the programmable thermal sensor within a single semiconductor chip, Sawtell does not disclose placing the programmable thermal sensor on a same chip as a microprocessor. *Thus applicant respectfully submits Sawtell does not teach or disclose generating a temperature signal within the microprocessor indicative of the temperature of the microprocessor.*

Matsuo discloses generating a temperature signal indicative of the temperature of a heat generating element. Matsuo also discloses a microprocessor that issues control signals depending upon the sensed temperature of the heat generating element. The heat generating element is distinct from the microprocessor itself. *Thus applicant respectfully submits Matsuo does not teach or disclose generating a temperature signal within the microprocessor indicative of the temperature of the microprocessor.*

Barrett does not include a disclosure of sensing a temperature of the microprocessor. *Thus applicant respectfully submits Barrett does not teach or disclose generating a temperature signal within the microprocessor indicative of the temperature of the microprocessor.*

In contrast, method claims 49, 51, and 54, as amended, include the language:

> 49. A method of controlling a temperature of a microprocessor, comprising the steps of:
> *a) generating a temperature signal within the microprocessor indicative of the temperature of the microprocessor;*

(Claim 49, as amended)(*emphasis added*)

> 51. A method of controlling a temperature of a microprocessor, comprising the steps of:
> *a) generating a temperature signal within the microprocessor corresponding to the temperature of the microprocessor;*

(Claim 51, as amended)(*emphasis added*)

> 54. A method of controlling a frequency of a clock signal which drives a microprocessor, comprising the steps of:
> *a) generating a temperature signal within the microprocessor corresponding to a temperature of the microprocessor;*

(Claim 54, as amended)(*emphasis added*)

Moreover, applicant respectfully submits that none of the cited references teach or discloses the method further comprising the steps of generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded and at least one of a) decreasing a microprocessor clock frequency in response to the interrupt signal, or b) activating an active cooling device to decrease the microprocessor temperature in response to the interrupt signal.

To the contrary, Sawtell does not teach or disclose decreasing microprocessor clock frequencies in response to any signals generated by the temperature sensor. Given that the claimed temperature signal corresponds to the temperature of the microprocessor and Sawtell does not teach or disclose measuring the temperature of a microprocessor, the signal generated by Sawtell cannot correspond to the claimed interrupt signal. Thus Sawtell does not teach or disclose activating an active cooling device to decrease the microprocessor temperature in response to the claimed interrupt signal.

Matsuo discloses generating a signals indicative of the crossing of temperature thresholds, but the signals are indicative of the temperature of a heat generating element - not the microprocessor. Moreover, Matsuo discloses providing a indication of failure or shutting off the power to the heat generating element rather than decreasing a microprocessor clock frequency in response to the interrupt signal. The active cooling device cools the heat generating element not the microprocessor of the control unit. The activation of the active cooling device is apparently controlled entirely independently of the microprocessor or the temperatures sensed by the microprocessor. *Thus Matsuo does not teach or disclose the method further*

comprising the steps of generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded and at least one of a) decreasing a microprocessor clock frequency in response to the interrupt signal, or b) activating an active cooling device to decrease the microprocessor temperature in response to the interrupt signal.

Barrett does not teach or disclose generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded. Although Barrett discloses sensing interrupt signals, the clock frequency is *increased* in response to interrupt signals, not decreased. Finally, although Barrett discloses active cooling devices, such as fans, Barrett teaches attempting to minimize their use by slowing the clock during wait states *independently of a temperature of the microprocessor. Thus Barrett does not teach or disclose the method further comprising the steps of generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded and at least one of a) decreasing a microprocessor clock frequency in response to the interrupt signal, or b) activating an active cooling device to decrease the microprocessor temperature in response to the interrupt signal.*

Thus none of the cited references, alone or combined, teaches or discloses the method further comprising the steps of *generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded and at least one of a) decreasing a microprocessor clock frequency in response to the interrupt signal, or b) activating an active cooling device to decrease the microprocessor temperature in response to the interrupt signal.*

In contrast, claims 49 and 51 include the language:

> 49. A method of controlling a temperature of a microprocessor, comprising the steps of:
> a) generating a temperature signal within the microprocessor indicative of the temperature of the microprocessor;
> b) comparing the temperature signal with a first threshold temperature level within the microprocessor;
> *c) generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded; and*
> *d) decreasing a microprocessor clock frequency in response to the interrupt signal.*

(Claim 49, as amended)(*emphasis added*)

> 51. A method of controlling a temperature of a microprocessor, comprising the steps of:
> a) generating a temperature signal within the microprocessor corresponding to the temperature of the microprocessor;
> b) comparing the temperature signal with a first threshold temperature level within the microprocessor;
> *c) generating an interrupt signal if the temperature signal indicates that the first threshold temperature level has been exceeded; and*
> *d) activating an active cooling device to decrease the microprocessor temperature in response to the interrupt signal.*

(Claim 51, as amended)(*emphasis added*)

For the reasons presented above, applicant respectfully submits that claims 49, 51, and 54 are patentable under 35 U.S.C. § 103 in view of the cited references.

Thus applicant respectfully submits independent claims 37, 43, 49, 51, 54, and 59 are patentable under 35 U.S.C. § 103.

Given that claims 38-42 depend from claim 37 and claims 44-48 depend from claim 43, claim 50 depends from claim 49, claims 52-53 depend from claim 51, claims 55-58 depend from claim 54, and claim 60 depends from

claim 59, applicant respectfully submits claims 38-42, 44-48, 50, 52-53, 55-58, and 60 are likewise patentable under 35 U.S.C. § 103 in view of the cited references.

Applicant respectfully submits the rejections under 35 U.S.C. § 103 have been overcome.

Conclusion

Applicant respectfully submits that in view of the arguments set forth herein, the applicable rejections and objections have been overcome. Accordingly, claims 37-60 should be found to be in condition for allowance.

If there are any issues that can be resolved by telephone conference, the Examiner is respectfully requested to contact the undersigned at **(503) 684-6200.**

An Information Disclosure Statement accompanies this response.

If there are any additional charges associated with this communication, please charge Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, L.L.P.

Date: June 27, 1997

William D. Davis

William D. Davis
Reg. No. 38,428

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(503) 684-6200